

Application Serial No. 10/624,340

### **In The Claims**

Claims 1-41, 52-63, and 71-78 are pending in the application with claims 42-51 and 64-70 cancelled herein.

1. (original) A capacitor construction comprising:  
a first electrode;  
a nitride layer between the first electrode and a surface supporting the capacitor construction;  
a capacitor dielectric over the first electrode; and  
a second electrode over the capacitor dielectric.
2. (original) The capacitor construction of claim 1 wherein the nitride layer is conductive.
3. (original) The capacitor construction of claim 2 wherein the first electrode is in conductive contact with the nitride layer.
4. (original) The capacitor construction of claim 3 exhibiting a lower RC time constant compared to an otherwise identical capacitor construction lacking the conductive nitride layer.
5. (original) The capacitor construction of claim 1 wherein the nitride layer comprises TiN.
6. (original) The capacitor construction of claim 1 wherein the nitride layer is insulative.

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7. (original) The capacitor construction of claim 6 wherein the first electrode is on the nitride layer.

8. (original) The capacitor construction of claim 1 wherein the first electrode comprises a conductive rough silicon layer.

9. (original) The capacitor construction of claim 8 wherein the first electrode further comprises another conductive layer over the rough silicon layer.

10. (original) The capacitor construction of claim 1 wherein the first electrode comprises Si and the nitride layer limits the Si from contributing to formation of metal silicide material between the first electrode and the supporting surface.

11. (original) The capacitor construction of claim 1 further comprising an undoped rough silicon layer between the first electrode and the nitride layer, the nitride layer limiting Si of the rough silicon layer from contributing to formation of metal silicide material between the rough silicon layer and the supporting surface.

12. (original) The capacitor construction of claim 1 wherein the nitride layer comprises silicon nitride.

13. (original) A capacitor construction comprising:  
a rough silicon layer;  
a nitride layer under the rough silicon layer;  
a capacitor dielectric over the rough silicon layer; and  
an electrode over the capacitor dielectric.

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14. (original) The capacitor construction of claim 13 wherein the nitride layer is conductive.

15. (original) The capacitor construction of claim 14 wherein the rough silicon layer is conductive, the nitride layer and the rough silicon layer being comprised by another electrode under the capacitor dielectric.

16. (original) The capacitor construction of claim 15 exhibiting a lower RC time constant compared to an otherwise identical capacitor construction lacking the conductive nitride layer.

17. (original) The capacitor construction of claim 13 wherein the nitride layer comprises TiN.

18. (original) The capacitor construction of claim 13 wherein the nitride layer is insulative.

19. (original) The capacitor construction of claim 18 wherein the rough silicon layer is on the nitride layer.

20. (original) The capacitor construction of claim 18 further comprising another electrode over the rough silicon layer and under the capacitor dielectric.

21. (original) The capacitor construction of claim 18 wherein the nitride layer comprises silicon nitride.

22. (original) The capacitor construction of claim 13 wherein the rough silicon layer is undoped.

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23. (original) The capacitor construction of claim 13 wherein the nitride layer limits Si of the rough silicon layer from contributing to formation of metal silicide material under the rough silicon layer.

24. (original) A capacitor construction comprising:  
a conductive rough silicon layer over a support surface;  
a nitride layer between the rough silicon layer and the support surface;  
a first electrode comprising the rough silicon layer;  
a capacitor dielectric over the first electrode; and  
a second electrode over the capacitor dielectric.

25. (original) The capacitor construction of claim 24 wherein the nitride layer is conductive.

26. (original) The capacitor construction of claim 25 wherein the first electrode further comprises the nitride layer.

27. (original) The capacitor construction of claim 26 exhibiting a lower RC time constant compared to an otherwise identical capacitor construction lacking the conductive nitride layer.

28. (original) The capacitor construction of claim 24 wherein the nitride layer comprises TiN.

29. (original) The capacitor construction of claim 24 wherein the nitride layer is insulative.

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30. (original) The capacitor construction of claim 29 wherein the first electrode further comprises another conductive layer between the rough silicon layer and the capacitor dielectric.

31. (original) The capacitor construction of claim 30 wherein the another conductive layer comprises TiN.

32. (original) The capacitor construction of claim 24 wherein the nitride layer comprises silicon nitride.

33. (original) The capacitor construction of claim 24 wherein the nitride layer limits Si of the rough silicon layer from contributing to formation of metal silicide material between the rough silicon layer and the support surface.

34. (original) A capacitor construction comprising:

a storage node in a substrate;

a composite first electrode comprising a first conductive layer over and in conductive contact with the storage node and comprising a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer;

a capacitor dielectric over the first electrode; and

a second electrode over the capacitor dielectric.

35. (original) The capacitor construction of claim 34 wherein the first conductive layer comprises a nitride.

36. (original) The capacitor construction of claim 34 exhibiting a lower RC time

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constant compared to an otherwise identical capacitor construction lacking the first conductive layer.

37. (original) The capacitor construction of claim 34 wherein the first conductive layer limits Si of the polysilicon layer from contributing to formation of metal silicide material between the polysilicon layer and the storage node.

38. (original) The capacitor construction of claim 34 wherein the first conductive layer does not substantially comprise silicon.

39. (original) The capacitor construction of claim 34 wherein the first conductive layer comprises TiN.

40. (original) The capacitor construction of claim 34 wherein the polysilicon layer comprises HSG silicon.

41. (original) The capacitor construction of claim 34 wherein the polysilicon layer is on the first conductive layer.

Claims 42-51 (cancelled).

52. (original) A capacitor construction forming method comprising:  
forming a nitride layer over a surface supporting the capacitor construction;  
forming a first electrode over the nitride layer;  
forming a capacitor dielectric over the first electrode; and  
forming a second electrode over the capacitor dielectric.

53. (original) The method of claim 52 wherein the nitride layer is conductive.

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54. (original) The method of claim 53 wherein the first electrode is in conductive contact with the nitride layer and the capacitor construction exhibits a lower RC time constant compared to an otherwise identical capacitor construction lacking the conductive nitride layer.

55. (original) The method of claim 53 wherein the first electrode comprises a conductive HSG silicon layer and another conductive layer over the HSG silicon layer.

56. (original) The method of claim 52 wherein the nitride layer is insulative.

57. (original) The method of claim 52 wherein the first electrode comprises Si and the nitride layer limits the Si from contributing to formation of metal silicide material between the first electrode and the supporting surface.

58. (original) The method of claim 52 further comprising forming an undoped HSG silicon layer between the first electrode and the nitride layer, the nitride layer limiting Si of the HSG silicon layer from contributing to formation of metal silicide material between the HSG silicon layer and the supporting surface.

59. (original) A capacitor construction forming method comprising  
forming a storage node in a substrate;  
forming a first conductive layer over and in conductive contact with the storage node;  
forming a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer and the first conductive layer and

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polysilicon layer being comprised by a composite first electrode;

forming a capacitor dielectric over the first electrode; and

forming a second electrode over the capacitor dielectric.

60. (original) The method of claim 59 wherein the first conductive layer comprises a nitride.

61. (original) The method of claim 59 wherein the capacitor construction exhibits a lower RC time constant compared to an otherwise identical capacitor construction lacking the first conductive layer.

62. (original) The method of claim 59 wherein the first conductive layer limits Si of the polysilicon layer from contributing to formation of metal silicide material between the polysilicon layer and the storage node.

63. (original) The method of claim 59 wherein the polysilicon layer is formed on the first conductive layer.

Claims 64-70 (cancelled).

71. (original) A memory device comprising a plurality of memory cells that have a capacitor including:

a first electrode;

a nitride layer between the first electrode and a surface supporting the capacitor construction;

a capacitor dielectric over the first electrode; and

a second electrode over the capacitor dielectric.

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72. (original) The memory device of claim 71 wherein the plurality of memory cells comprises an array of memory cells and the memory device comprises DRAM.

73. (original) A memory device comprising a plurality of memory cells that have a capacitor including:

a storage node in a substrate;

a composite first electrode comprising a first conductive layer over and in conductive contact with the storage node and a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer;

a capacitor dielectric over the first electrode; and

a second electrode over the capacitor dielectric.

74. (original) The memory device of claim 73 wherein the plurality of memory cells comprises an array of memory cells and the memory device comprises DRAM.

75. (original) A computer system, the computer system comprising a memory device and a microprocessor, the memory device including:

a first electrode;

a nitride layer between the first electrode and a surface supporting the capacitor construction;

a capacitor dielectric over the first electrode; and

a second electrode over the capacitor dielectric.

76. (original) The computer system of claim 75 wherein the memory device comprises DRAM.

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77. (original) A computer system, the computer system comprising a memory device and a microprocessor, the memory device including:

a storage node in a substrate;

a composite first electrode comprising a first conductive layer over and in conductive contact with the storage node and a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer;

a capacitor dielectric over the first electrode; and

a second electrode over the capacitor dielectric.

78. (original) The computer system of claim 77 wherein the memory device comprises DRAM.